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Letter

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Low-Voltage Flexible Organic Electronics Based on High-Performance Sol–Gel Titanium Dioxide Dielectric

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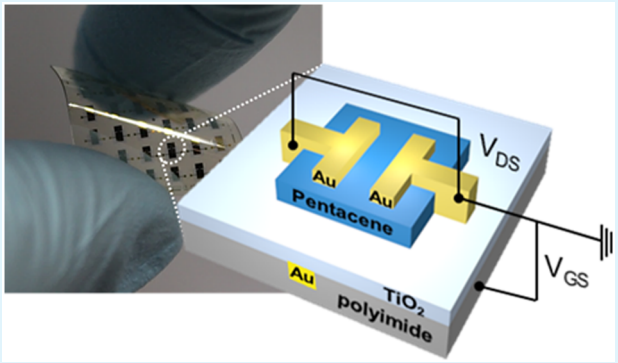
Supporting Information

ABSTRACT: In this letter, we report that high-performance insulating films can be generated by judicious control over the microstructure of sol–gel-processed titanium dioxide (TiO_2) films, typically known as wide-bandgap semiconductors. The resultant device made of 23 nm-thick TiO_2 dielectric layer exhibits a low leakage current density of $\sim 1 \times 10^{-7}$ A cm^{-2} at 2 V and a large areal capacitance of 560 nF cm^{-2} with the corresponding dielectric constant of 27. Finally, low-voltage flexible organic thin-film transistors were successfully demonstrated by incorporating this versatile solution-processed oxide dielectric material into pentacene transistors on polyimide substrates.



KEYWORDS: *titanium dioxide, sol–gel, gate dielectric, low-voltage, organic thin-film transistor*

Organic thin-film transistors (OTFTs) find their broad technological implications in flat-panel displays, active-matrix imagers, and biochemical sensors. From the material point of view, much effort has been devoted to the development and engineering of organic semiconductors that constitute the active part of electrical devices.[1] On the other hand, the performance and processability of gate-dielectric materials, particularly for OTFTs, has received relatively little attention, whereas they possess grave importance for reducing both the operation voltage and power consumption upon practical usage.[2−4]

Recently, titanium dioxide (TiO_2) has received considerable attention because of their intriguing optoelectronic properties.[5,6] This unique oxide material has been employed as a promising photocatalyst platform because it exhibits wide-bandgap semiconducting properties, solution processability, and facile photoactivation suitable for dye-sensitized solar cells (DSSCs), perovskite-based hybrid photovoltaics, and photoelectrochemical cells.[7−9] Furthermore, the electron–hole pair generation upon ultraviolet light irradiation and subsequent reactive radical formation in the presence of oxygen and water has been successfully utilized for the photoinduced self-cleaning coatings based on TiO_2.[10]

However, there have been only a small number of scientific reports on thin-film transistors (TFTs) based on TiO_2 either as a semiconductor or dielectric. Although the vast majority of previous reports employed TiO_2 as a channel material,[11−13] there has been some insight that its high permittivity could be promising for the purpose of TFT gate dielectric.[14] Nonetheless, it has been challenging to realize an optimal dielectric performance due to the trade-off between the mechanical and electrical properties related to the thermal process. Sol–gel metal oxide films typically require a high-temperature annealing step for near-complete polycondensation and film densification; such a process results in a mechanically dense film with a high dielectric constant, ideal for reducing the operation voltage of TFTs.[15] However, we noticed that an elevated temperature induces semiconducting crystalline phase of an oxide film, which negatively affects the electrical insulation in a final device architecture. This aspect partially explains why a pristine, single-layer TiO_2 gate dielectric has barely been reported in the community; hybrid composite formation with or additional barrier deposition of polymeric insulating materials (e.g., polyvinylphenol, polystyrene, etc.) were utilized to decrease the apparently high leakage current.[16−18] However, it is important to note that the use of such composite/multilayer structures for minimizing leakage current sacrifices both the simplicity in fabrication and the inherent high permittivity of TiO_2 material. We found an example of organic TFTs (OTFTs) with a TiO_2-only dielectric layer in the previous literature;[19] however, the consequent device performance was

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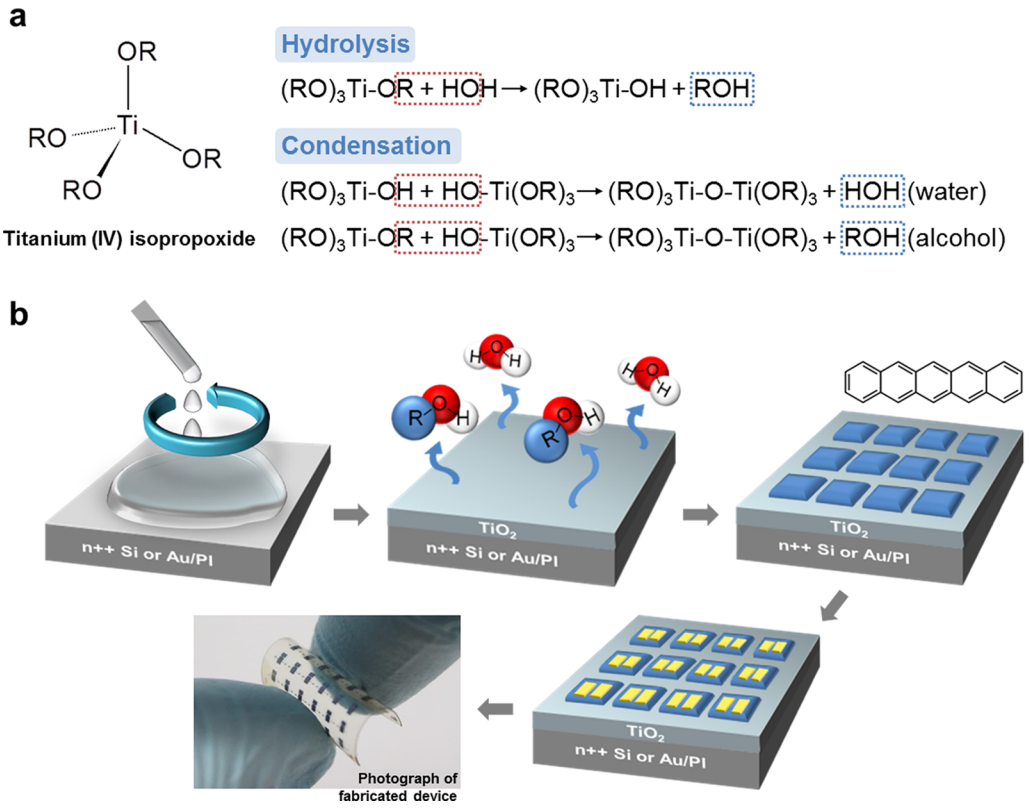
Scheme 1. (a) Chemical Equations of Hydrolysis and Polycondensation Reactions in a Sol–Gel-Based Titanium(IV) Isopropoxide Precursor Solution, and (b) the Fabrication of the Pentacene Thin Film Transistors with Solution-Processed TiO_2 as Gate Dielectrics



not outstanding, possibly because of the low film quality of their relatively thick (130 nm) solution-processed dielectric.

Herein, we demonstrate that the moderately high thermal annealing of sol–gel TiO_2 material enables the formation of excellent dielectric films with high dielectric constant and low leakage current density out of the sol–gel oxide material typically known as a semiconductor. The judicious control of TiO_2 film microstructure via minute thermal manipulation was executed and the corresponding changes in sol–gel oxide film properties were investigated via extensive thermal, chemical, and film-microstructure analyses to understand the consequent device characteristics in low-voltage flexible OTFTs.

Sol–gel titanium dioxide films were formed using a 0.2 M titanium(IV) isopropoxide solution in 2-methoxyethanol (2-ME), which were stirred for 12 h while being heated at 75 °C before film deposition. Because of the moisture sensitivity, anhydrous solvent was employed and precursor solutions were prepared inside a nitrogen-filled glovebox under strictly controlled humidity. First, titanium alkoxide undergoes partial hydrolysis and condensation by reacting with residual water in a precursor solution (Scheme 1).[20] After film deposition, the initially xerogel-like oxide film becomes densified via formation of metal–oxygen–metal (i.e., Ti–O–Ti) network and evaporation of condensation byproducts (i.e., water and alcohol), whereas the further condensation among the unreacted hydroxyl groups is going on during a postannealing step. X-ray photoelectron spectroscopy (XPS) data in the energy range of Ti 2*p* and O 1*s* electrons (see Figure S1 in the Supporting Information) show the deconvoluted peaks at 464.6 and 458.8 eV which correspond to the electron binding energy of Ti $2p_{1/2}$ and $2p_{3/2}$, respectively. This XPS profile confirms that the titanium dioxide with the Ti oxidation state of +4 is formed in our experimental condition.[21,22] The intensity profile of O 1*s* peaks at 530.4 eV (Ti–O–Ti, ~81%) and 531.9 eV (Ti–O–H, ~19%) indicates that the most of Ti–OH functionality is transformed to Ti–O–Ti via efficient condensation process.[23,24] Nonetheless, the unreacted Ti–OH residues inside the titanium dioxide film might be the possible origin of small hysteresis in TFT device characteristics (vide infra).

To monitor the change in sol–gel film properties depending on the annealing temperature, thermogravimetric analysis (TGA) was performed with partially condensed sol–gel oxide powders, which were prepared by evaporating 2-ME out of the stirred precursor solution at room temperature overnight. As shown in the TGA plot (Figure 1a), the first weight loss starts at 80 °C, which is attributed to the evaporation of residual solvent, 2-ME, and subsequently, the second one starts at 250 °C, which is attributed to the removal of condensation byproducts (i.e., water and isopropyl alcohol).[25] Note that at low annealing temperatures these small molecules can be trapped inside the sol–gel oxide matrix as impurities and the incomplete condensation can lead to poor film densification. Therefore, we argue that the thermal annealing below 250 °C presumably produces the poorly insulating TiO_2 films (vide infra). The similar courses of condensation and densification at different temperatures are confirmed by attenuated total reflectance Fourier transform infrared (ATR-FTIR) spectroscopy. In Figure 1b, the broad absorption bands around 3300 and 1640 cm^{-1}, which are ascribed to O–H stretching and water O–H bending, respectively, appear prominent up to 150

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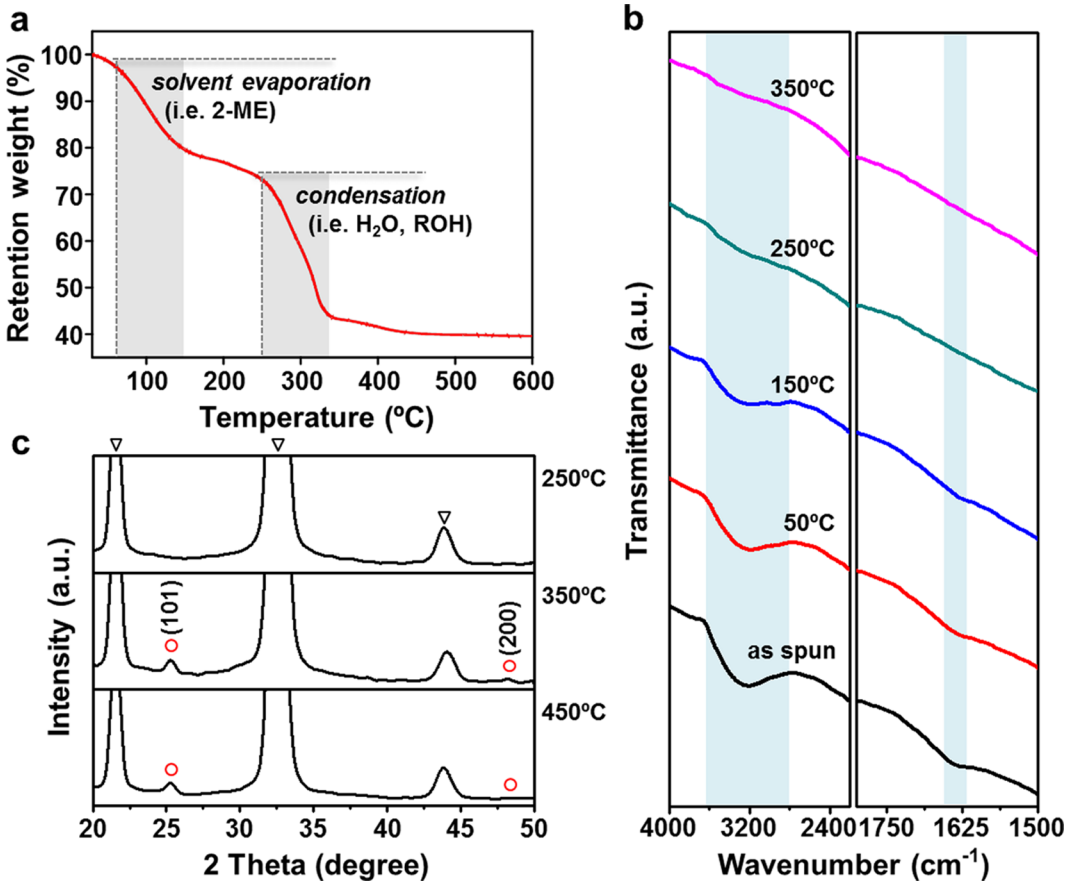

Figure 1. Thermal, chemical, and microstructural analyses of thermally processed sol–gel TiO_2 films. (a) TGA plot in the range of 30 to 600 °C, (b) ATR-FTIR spectra, and (c) XRD diffractograms of the TiO_2 films annealed at different temperatures (the inverted triangle (∇) marks indicate the silicon substrate peaks).

°C; however, these bands begin to disappear once the annealing temperature of the as-deposited film is raised above 250 °C.

It is well-known that anatase or rutile is formed from the solution-processed TiO_2 material at high annealing temperatures (typically above 500 °C).[26,27] Such a crystalline region contributes leakage current pathway and is less preferred for the insulator purpose. Figure 1c shows a series of X-ray diffractogram (XRD) of TiO_2 films annealed at different temperatures between 250 and 450 °C. Thick TiO_2 films were deposited onto Si (100) substrates using 0.8 M solution of titanium(IV) isopropoxide in 2-ME to improve the signal-to-noise ratio in XRD data. No crystalline TiO_2 peak was detected in the film annealed at 250 °C, indicating that the resultant TiO_2 film is still amorphous. On the other hand, the diffractograms of those annealed at 350 and 450 °C show the crystalline peaks at the 2θ of 25 and 48°, which are ascribed to the anatase (101) and (200) phases, respectively.[28]

In parallel, transmission electron microscopy (TEM) analysis was carried out to confirm the local growth of anatase phase at high postannealing temperatures. Figure 2a, b shows the representative cross-sectional TEM images of sol–gel titanium dioxide films annealed at 250 and 350 °C. All the solution-deposited oxide films exhibit a highly densified cross-section as well as a uniform film thickness of 23 nm, and a well-defined interfacial boundary with native silicon dioxide. Unlike that annealed at 250 °C with no apparent crystallinity, the oxide film annealed at 350 °C clearly shows the scattered partial crystallization, which is also confirmed by the electron

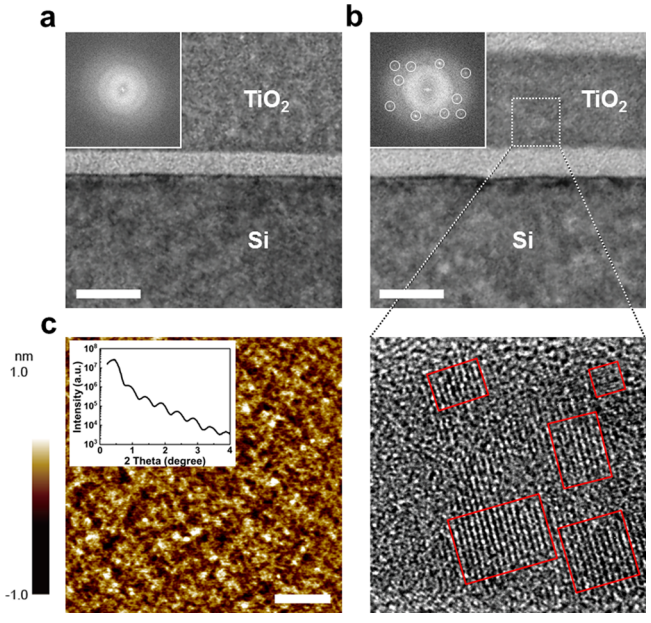

Figure 2. Cross-sectional TEM images of sol–gel TiO_2 films annealed at (a) 250 °C and (b) 350 °C, with the electron diffraction patterns in Fourier-transformed images (inset). (c) AFM image of the film annealed at 250 °C with X-ray reflectivity data (inset) (scale bars denote 10 nm and 1 μm in TEM and AFM images, respectively).

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diffraction patterns in Fourier-transformed images. The atomic force microscopy (AFM), X-ray reflectivity (XRR), and scanning electron microscopy (SEM) data visualize very smooth surface (root-mean-square roughness of 0.17 nm) and featureless surface morphology indicating the absence of crystallinity in the 250 °C-annealed film (Figure 2c and Figure S2 in the Supporting Information). All the aforementioned film characterizations (i.e., TGA, XRD, FTIR, TEM, AFM, and XRR) lead to the conclusion that the annealing temperature of sol–gel TiO_2 films needs to be at least around 250 °C for near-complete condensation and film densification; however, it needs to be below 350 °C for the least crystalline formation.

Low leakage current density and high areal capacitance are two essential requirements guaranteeing the excellent gate-dielectric performance for the TFT application. The former is related to the high film density as well as the minimized impurity inclusion and the latter the reduced film thickness with high dielectric constant. The electrical devices using thermally annealed TiO_2 films were characterized to verify the correlation between film properties and electrical performance. For device fabrication, amorphous TiO_2 films were deposited onto precleaned n^{++}-silicon substrates by spin-coating and the top electrodes were defined by thermal evaporation of 40 nm thick gold films through a shadow mask. Figure 3a shows the plots of current density–voltage and areal capacitance-frequency where each data point represents a statistically averaged value. These metal–insulator–semiconductor (MIS) capacitors with a TiO_2 dielectric layer annealed at 250 °C exhibit a low current density of $\sim 1 \times 10^{-7}$ A cm^{-2} at 2 V and a high areal capacitance of 560 nF cm^{-2} at 10 kHz. These devices contain 23 nm-thick TiO_2 and 3 nm-thick native SiO_2 layers as confirmed by spectroscopic ellipsometry and cross-sectional TEM. With two parallel-plate capacitors in series assumed, the dielectric constant of TiO_2 layer was estimated as 27. It is worth mentioning that the sol–gel TiO_2 dielectrics annealed at 350 °C exhibit the larger leakage current density and pronounced device-to-device variation (Figure 3b), which can be explained by the onset of local crystallization (Figure 2b). Therefore, we suppose that the precautious temperature control during thermal annealing step affords highly dense, smooth, non-crystalline TiO_2 films with reliable insulating performance and high dielectric constant.

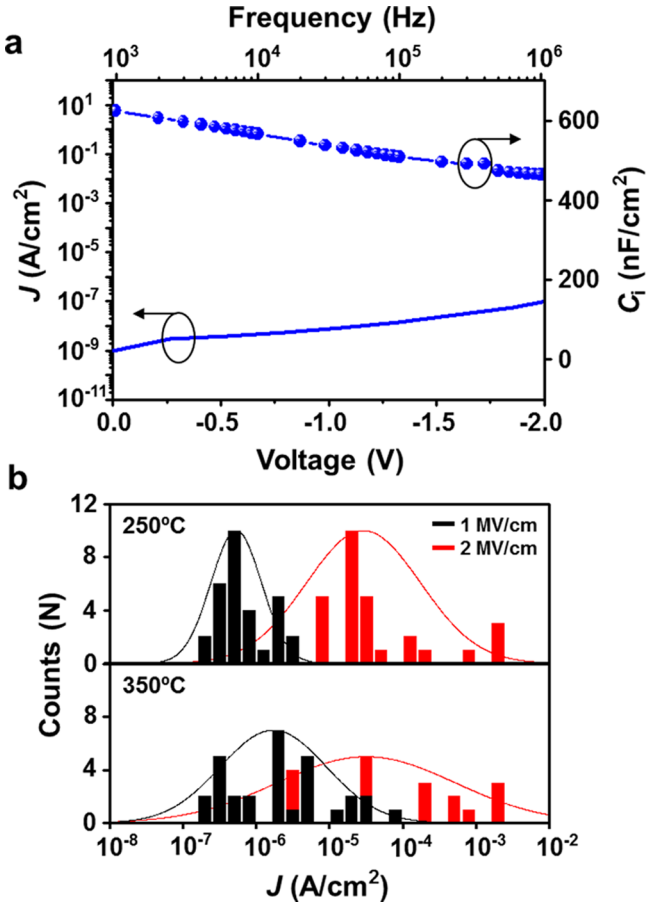

Figure 3. (a) Current density–voltage (J–V) and areal capacitance-frequency (C–f) plots averaged over MIS devices using a TiO_2 dielectric film annealed at 250 °C. (b) Statistical variation of the leakage current density in the TiO_2 dielectric films annealed at 250 (upper) and 350 °C (lower).

The low-voltage OTFTs benefiting from the high performance dielectric was demonstrated by incorporating the amorphous titanium dioxide layer into pentacene-based transistors. First, XRD and AFM studies confirmed that the typical polycrystallinity, dendritic growth pattern, and terrace-like morphology of the vacuum-deposited pentacene film (50 nm thick) are not affected by the underlying TiO_2 layer (Figure 4a). Output and transfer characteristics of the OTFTs fabricated on rigid substrates are shown in Figure 4b and c, respectively. Due to the reduced film thickness and high dielectric constant value of the TiO_2 dielectric layer, the low-voltage operation of pentacene TFTs with low gate leakage current is successfully demonstrated. A representative TFT transfer curve exhibits the extracted field-effect mobility (μ) of 0.07 cm^2 V^{-1} s^{-1}, the current on/off ratio of $\sim 1 \times 10^4$, the threshold voltage (V_T) of −0.3 V, and the subthreshold swing (SS) of 170 mV/decade. The relatively low value of channel mobility and the appearance of hysteresis in transfer sweep are ascribed to the existence of residual hydroxyl group in the dielectric layer interfacing with pentacene film (Figure S1 in the Supporting Information). It is expected that charge transport in the TFT channel can be improved by chemical passivation of TiO_2 dielectric surface with a self-assembled monolayer of alkylphosphonic acid.[29,30]

Finally, because of the moderately high annealing temperature and the mechanical flexibility of amorphous thin TiO_2 dielectric films, low-voltage flexible pentacene transistor arrays were successfully fabricated on plastic substrates as shown in Figure 4d. Here, polyimide (PI) films were chosen because of their outstanding thermal stability and high glass transition temperature (T_g > 300 °C). A fabricated flexible device shows the μ of 0.12 cm^2 V^{-1} s^{-1}, the current on/off ratio of $\sim 1 \times 10^4$, V_T of −0.2 V, and SS of 180 mV/decade. Note that the performance metrics of the flexible pentacene TFT on PI are comparable to those of the TFTs on rigid silicon substrate. It is noteworthy that the aforementioned insulating properties of the TiO_2-based dielectric films and TFT characteristics were achieved without additional insulating barrier deposition on the bare TiO_2 layer.[19] These results suggest that the solution-processed amorphous TiO_2 film is an excellent dielectric material compatible with both organic semiconductors and mechanically flexible substrates.

In conclusion, we successfully fabricated pentacene TFTs with solution-processed TiO_2 material as a gate dielectric. Through exhaustive film characterizations, the optimal thermal annealing condition was investigated to enable the formation of

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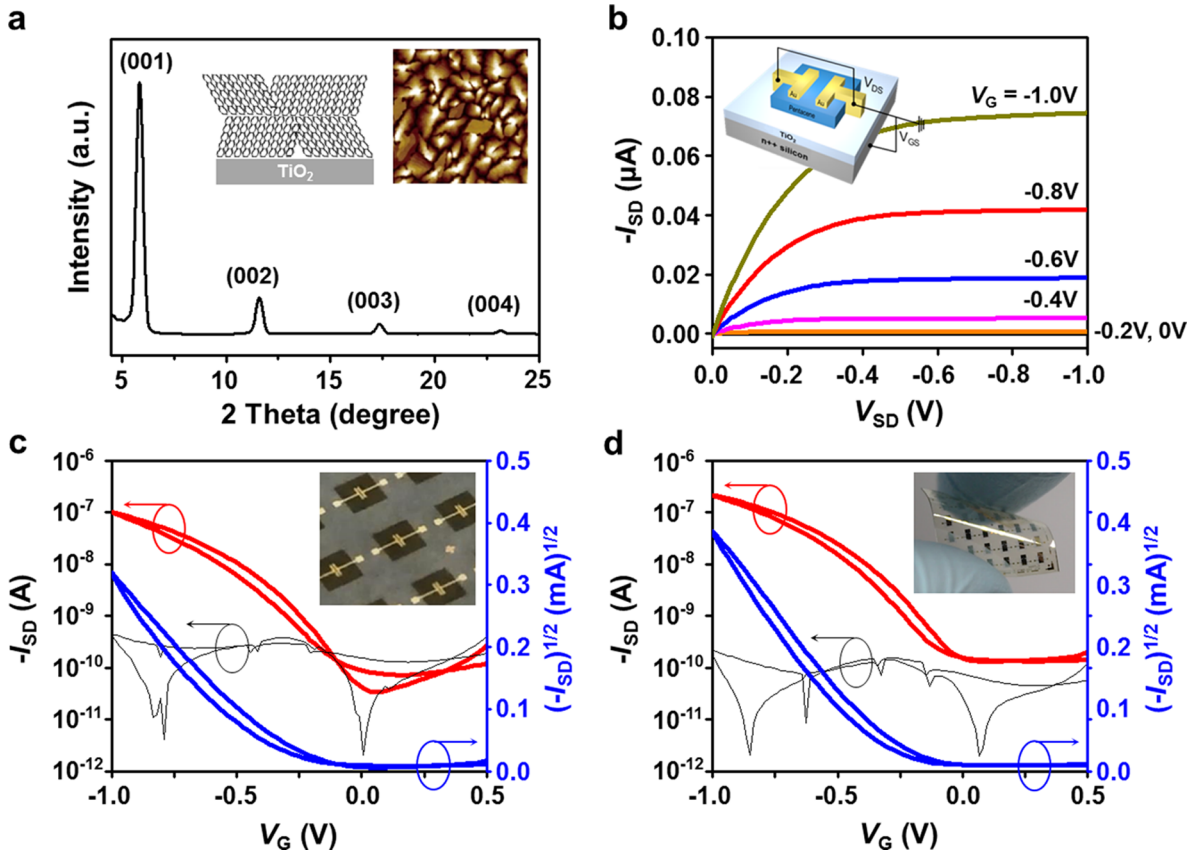

Figure 4. (a) XRD spectra and AFM image of a vacuum-evaporated pentacene film on amorphous TiO_2 film. (b) Output characteristics at various V_G values and (c) a transfer characteristic at V_{SD} = −0.5 V of a pentacene-TiO_2 TFT on a rigid silicon substrate. (d) Transfer characteristic at V_{SD} = −0.5 V of a pentacene-TiO_2 TFT on a flexible polyimide substrate.

amorphous, smooth, densified TiO_2 films from a sol−gel precursor solution. The sol−gel TiO_2 film deposition and subsequent thermal treatment at 250 °C lead to the highly dense amorphous thin oxide layer with outstanding dielectric properties even without additional insulating barrier. Finally, thin TiO_2 films were successfully incorporated into the pentacene-based TFTs both on rigid and flexible substrates for low-voltage device operation. We expect that the solution-processed amorphous TiO_2 film is a very useful dielectric material for realizing high-performance, transparent, flexible organic electronics with low-voltage operation and large-area processability at affordable cost.

■ ASSOCIATED CONTENT

Supporting Information

The experimental details on preparation and characterization of sol−gel films and corresponding devices are available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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